

- 1 -

METHOD AND APPARATUS OF DATA TRANSMISSION

CROSS-REFERENCES TO RELATED APPLICATIONS

The present invention relates to the following U.S. Patent application assigned to the assignee of the present invention. U.S. Serial No. 09/099390,

5 Atushi Miyasita et al. filed on June 18, 1998 entitled "OFDM MODULATOR AND OFDM MODULATION METHOD FOR DIGITAL MODULATED WAVE HAVING GUARD INTERVAL", U.S. Serial No. 09/096454, Seiichi Sano et al. filed on June 11, 1998 entitled "DATA TRANSMISSION APPARATUS AND RECEIVING

10 APPARATUS USING ORTHOGONAL FREQUENCY DIVISION MULTIPLEX MODULATION SYSTEM" and U.S. Serial No. 09/203564, Seiichi Sano et al. filed on December 2, 1998 entitled "SYNCHRONIZATION DETECTION METHOD FOR DATA TRANSMISSION APPARATUS AND DATA TRANSMISSION APPARATUS USING THE

15 SAME".

BACKGROUND OF THE INVENTION

The present invention relates in general to a method and an apparatus for transmitting data, and more particularly to a method and an apparatus for transmitting data employing an OFDM (Orthogonal Frequency Division Multiplex) system, and a method and an apparatus for receiving an OFDM signal.

In recent years, as for the modulation method which is suitable for being applied to the digital

audio broadcasting for mobiles and terrestrial digital television broadcasting, the OFDM system which features a robustness to multi path fading and ghost has received much attention. The OFDM system is one of the 5 multi-carrier modulation systems and is a transmission method of subjecting n carriers (n is in the range of several tens to several hundreds) which are authogonal to one another.

Then, as shown in Fig. 2, the modulated 10 signal is transmitted which is acquired by adding a large number of digital modulated waves to one another and by subjecting the I-axis and the Q-axis to the orthogonal modulation. While as for the above-mentioned digital modulation method, in general, the 4 15 DQPSK (4 Differential Quadrature Phase Shift Keying) system is often employed, it is also possible to employ the multi-value modulation system such as the 16 QAM (16 Quadrature Amplitude Modulation) or the 32 QAM.

In addition, as shown in Fig. 3, the symbol 20 of the OFDM is constructed such that the guard interval for reducing the influence of the delayed wave is added to the effective data symbol. The guard interval is the signal which is added cyclically to the signal of the effective data symbol. The guard interval is 25 described in, for example, U.S. Serial No. 09/099390 (corresponding to European Patent application No. 98111075.2 filed on June 17, 1998) entitled "OFDM MODULATOR AND OFDM MODULATION METHOD FOR DIGITAL

MODULATED WAVE HAVING GUARD INTERVAL", the disclosure of which is hereby incorporated herein by reference.

By adding the guard interval, degradation due to the inter-symbol interference thereof can be avoided

5 against the delayed wave generated due to the delay time within the guard, and hence the OFDM system is robust to multi path fading.

On the other hand, since in the OFDM system, the frequency interval between the carriers is narrow,

10 interference between the carriers due to the carrier frequency error between the transmitter and the receiver and due to the sampling clock frequency error of the demodulation system may readily occur, and hence high accuracy is required for those frequencies.

15 For this reason, in order that the receiver may continue to receive properly the OFDM signal, there is required the processing of recovering the sampling clock with which the sampling clock frequency of the receiver is made coincide with the sampling clock frequency of the transmission signal. In addition, in the case where the frame period and the symbol period of the received signal fluctuate with time, the sampling clock frequency of the receiver needs to follow that fluctuation.

20 25 For this reason, the transmission side transmits the OFDM transmission signal in which the transmission frame is constituted by the effective data symbol and the several kinds of synchronous symbol

groups. An example of the constitution of the transmission frame is shown in Fig. 4.

The reception side executes the sync pull-in processing on the basis of the synchronous symbol.

5 Then, the sampling clock frequency on the transmission side is synchronized with the sampling clock frequency on the reception side to demodulate the OFDM signal.

In this connection, a prior art technique relating to sync pull-in based on the synchronous 10 symbol or the like is disclosed in JP-A-7-321762 for example.

SUMMARY OF THE INVENTION

First, description will hereinbelow be given with respect to an example of a configuration of an 15 OFDM digital transmission apparatus to which the present invention is applied and the operation thereof.

Fig. 5 is a block diagram showing a configuration of a transmitter for transmitting therefrom the above-mentioned transmission frame. The configuration 20 and operation of this transmitter will now be described with reference to Figs. 5 and 4, respectively.

As shown in Fig. 4, a first symbol is a null signal synchronous symbol (hereinafter, referred to as "a null symbol" for short, when applicable) and is 25 generated in a null symbol generator 54. The null symbol is zero on I and Q axes with respect to the amplitude thereof, and hence the null symbol is the

symbol for detecting roughly a specific position on the time base.

A second symbol is a symbol in which the amplitude is fixed, and the frequency thereof is

5 changed at fixed rate with time from the lower frequency to the upper frequency within the transmission band over the symbol period of time (hereinafter, referred to as "a sweep symbol" for short, when applicable) and is generated in a sweep symbol

10 generator 55. The auto-correlation function of this sweep symbol has a sharp peak value, and hence by utilizing this property, it is possible to acquire a specific time point on the time base with higher accuracy than that of the null symbol.

15 The symbols on and after a third symbol are constituted by data symbols with which the effective data is transmitted, and the data symbols of several tens to several hundreds of symbols are continuous therein. The data symbol is used to subject the data

20 mapped in a constellation mapping unit 51 to the IFFT (Inverse Fast Fourier Transform) arithmetic operation in an IFFT arithmetic operation unit 52 to convert the resultant data into a time base signal.

In a guard interval addition unit 53, the

25 guard interval is added to the signal from the IFFT arithmetic operation unit 52 to generate a data symbol of the OFDM signal.

The transmission frame is constituted by the

synchronous symbol and the data symbols, and a base band OFDM signal in a frame construction is outputted from a selector 56.

After being inputted to a D/A conversion unit 57 for digital/analog conversion therein, the OFDM signal is up-converted into the signal having an IF (Inter Frequency) band in a base band (BB)/IF conversion unit 58. Then, the OFDM transmission signal is transmitted in transmission frames.

Fig. 6 is a block diagram showing a configuration of a receiver for receiving the above-mentioned OFDM signal.

In the receiver shown in Fig. 6, after the received signal is converted into the signal having the IF band width, the signal having the IF band width is converted into the signal having the frequency band of the base band in an IF/BB conversion unit 61 to acquire the base band OFDM signal. Then, the base band OFDM signal is sampled using the sampling clock from a VCO 67 in an A/D conversion unit 62 to acquire the signal of the reception sample value sequence.

Next, description will hereinbelow be given with respect to the reception side sampling clock recovery processing wherein the sampling clock frequency when carrying out the sampling in the A/D conversion unit 62 is made coincide with the sampling clock frequency of the transmission signal, and a series of processing wherein the transition points of

the frame and the symbol of the reception sample value sequence signal are detected to control the timing of the frame and the symbol period of time in the receiver with reference to Fig. 8.

5 Fig. 8 is a time chart for explaining the operation of a frame counter 68.

The above-mentioned frame timing and symbol timing are counted in reception sampling clocks at an RES terminal of the frame counter 68.

10 First, as a first stage, a null symbol detection unit 63 detects a starting point of the null symbol from the reception sample value sequence signal sent from the A/D conversion unit 62 to output a signal NS exhibiting the rough starting point of the transmission frame. The signal NS is inputted to the frame counter 68 and resets the count value of the frame counter 68 at a time TC1.

15 The frame counter 68 continues to carry out the counting in reception sampling clocks to determine roughly the timing of the current frame and symbol.

20 In a second stage, since the information relating to the starting point of the frame detected by the null symbol detection unit 63 contains an error, the specific time point on the time base of the transmission frame is more accurately detected. For this reason, a time window having a predetermined length is provided on the time base on the basis of the null symbol starting position acquired in the first stage.

That is, this time window is initially provided a predetermined distance away from the null starting position on the time base. In general, the length of the time window has a length containing therein the 5 sweep symbol signal.

A sweep symbol correlation arithmetic operation unit 64 carries out the arithmetic operation of the cross-correlation between the received sample value sequence contained in that time window and the 10 sweep symbol signal, which is previously stored, every position of the time window while moving successively the time window from the initially set position on the time base to operate arithmetically a cross-correlation value sequence signal. In this connection, the time 15 window is moved by about more than ten samples before and after the sweep symbol in such a way as to contain at least the sweep symbol period of time of the received signal.

Since the sweep symbol is such that the auto- 20 correlation function has a sharp peak value, when the received sweep symbol coincides with the sweep symbol previously stored, the correlation value becomes a large value, while when the received sweep symbol is shifted therefrom on the time base, the correlation 25 value becomes almost zero. The cross-correlation value sequence which is acquired when moving the time window in this way is as shown in Fig. 7.

Next, a correlation maximum position detec-

tion unit 65 detects the maximum value from the cross-correlation value sequence. The correlation maximum value becomes maximum when the position of the time base coincides with the position of the sweep symbol in 5 the received signal.

Then, the correlation maximum position detection unit 65 operates arithmetically in reception sampling clocks an error on the time base between the position of the time window when outputting the 10 correlation maximum value and a time point of the sweep symbol which is counted on the basis of the null symbol starting position which has been detected in the first stage to output error information ERR.

Since the correlation maximum value position 15 detection unit 65 can detect the sweep symbol position in the reception sample value sequence with high accuracy, the detection unit 65 inputs the error information ERR acquired in the correlation maximum value position detection unit 65 to an LD terminal of 20 the frame counter 68 at a time TC3 to correct the count value. With respect to the correction of the count value, for example, the count value at a time point TC3 is corrected back and forth by the value of the error information ERR, whereby the frame timing of the 25 reception sample value sequence at a starting time point (TC4) of a next frame coincides with the frame timing of the frame counter 68.

In addition, that error information ERR is a

value acquired by counting in reception sampling clocks
an error in time between one frame period of time
counted using the sampling clock on the transmission
side and one frame period of time counted using the
5 reception sampling clock, and is converted into the
frequency error of the received sampling clock.

For this reason, a VCO control unit 66
outputs a signal which is used to control variably the
output clock frequency of a VCO 67 on the basis of the
10 error information ERR from the correlation maximum
value position detection unit 65. Then, the VCO 67
outputs the sampling clock variably controlled on the
basis of the frequency control signal from the VCO
control unit 66.

15 This frequency control is carried out an and
after the third frame similarly thereto, whereby the
sampling clock with which the received OFDM signal is
sampled can be synchronized with the clock on the
transmission side at all times.

20 In addition, after the frequency control for
the reception sampling clock has been roughly stabi-
lized as in a fourth frame of Fig. 8, in the case where
the value of the reception sampling error information
ERR falls within a predetermined range (within ± 1 for
25 example) in such a way that a slight error of the
reception sampling clock frequency does not reflect the
count value of the frame counter 68, the correction for
the count value is not carried out at all. This reason

is that since the control for the reception sampling clock frequency is carried out in samples, the error of the reception sampling clock frequency can not be controlled within ± 1 clock in one frame.

5 By executing the above-mentioned processing, since the reception sample value sequence is synchronized with the count value of the frame counter 68, it is possible to be accurately aware of a specific time point such as a transmission point of the frame or the
10 symbol on the reception sample value sequence.

Next, description will hereinbelow be given with respect to the processing of regenerating the reception sampling clock, and demodulation processing after the control for the frame timing and the symbol
15 timing has been established with reference to Fig. 6 and Figs. 9 to 11.

Fig. 9 is a diagram showing the relation between the FFT time window of the FFT arithmetic operation unit 69 and the symbol, Fig. 10 is a diagram
20 showing a relation between a principle wave and a reflected wave when the delay time of the reflected wave is shorter than the guard interval, and Fig. 11 is a diagram showing the relation between the principle wave and the reflected wave when the delay time of the
25 reflected wave is longer than the guard interval. In this connection, in Figs. 10 and 11, the height of the rectangle showing the principle wave for one symbol period and the height of the rectangle showing the

reflected wave for one symbol period represent schematically the relation between the reception intensity of the principle wave and that of the reflected wave. That is, in each of Figs. 10 and 11, 5 since the height of the rectangle of the principle wave is higher than that of the rectangle of the reflected wave, it is shown that the reception intensity of the principle wave is larger than that of the reflected wave.

10 In Fig. 6, first, the reception sample value sequence signal from the A/D conversion unit 62 is inputted to an FFT (Fast Fourier Transform) arithmetic operation unit 69.

Since the timing when the reception sample 15 value sequence signal is inputted to the FFT arithmetic operation unit 69, i.e., the time window of the FFT utilizes generally the guard interval effectively, as shown in Fig. 9, it is the timing when the reception sample value sequence of the backward period of time 20 (the effective data symbol unit) of the symbol is inputted, i.e., the time window thereof.

Now, since the OFDM modulated signal has the guard interval, as shown in Fig. 10, even if the reflected wave generated due to the presence of a 25 mountain or building is inputted, the longitudinal symbol is not mixed therewith at all as long as the delay time falls within the guard interval period of time.

However, as shown in Fig. 11, in the case where there is present the reflected wave having the delay time which is longer than the guard interval period of time, the front symbol is mixed therewith so 5 that the inter-symbol interference is generated.

In other words, since the inter-symbol interference in the OFDM signal is regarded as a mixing of Gaussian random noise, as a result, it appears in the form of the degradation of a C/N (Carrier/Noise) ratio 10 so that the code error rate is degraded.

Now, the data (reception sample value sequence signal) inputted to the FFT arithmetic operation unit 69 is subjected to Fast Fourie Transform for conversion from the time base signal to the frequency 15 base signal.

Then, a demodulation processing unit 6A demodulates the data, which has been converted into the frequency base signal in the FFT arithmetic operation unit 69, on the basis of the demodulation method corresponding to the modulation method every carrier to 20 output the demodulation result.

By executing the above-mentioned processing, it is possible to carry out the digital signal transmission employing the OFDM modulation method.

25 Let us consider the transmission under the condition of the transmission path of very poor quality such as in the mobile transmission in the case where the transmission is carried out using the transmitter

and the receiver according to the above-mentioned prior art.

Since in such a transmission path, the principle wave which is directly propagated from the 5 transmitter to the receiver, and the various kinds of reflected waves which have been reflected by buildings, mountains or the like are propagated with the respective predetermined delay times brought, the composite wave thereof is received at the receiver.

10 In addition, in the mobile transmission, the delay times or the levels of such reflected waves fluctuate every movement and further the principle wave is blocked by a building or the like so that the level of the principle wave may become small and hence each 15 of the levels of the reflected waves may be larger than than of the principle wave.

On the other hand, in the fixed line transmission, since in general, line-of-sight locations from the transmitter to the receiver is selected in order to 20 carry out the line design, the principle wave having a high level is stably present and hence it is rare that the transmission line condition becomes as poor as that of the mobile transmission.

However, in the case of the SFN (Single 25 Frequency Network) method wherein transit transmission is carried out using the same frequency in a plurality of switching offices, the composite wave of the two signals each having a high level due to the propagation

delay time difference in the propagation will be received in the vicinity of the intermediate point between one switching office and another switching office.

5 In this case, the signal which has reached formerly the receiver can be regarded as the principle wave, while the signal which has reached lately the receiver can be regarded as the reflected wave.

Examples of the arithmetic operation of the
10 value of the cross-correlation between the sweep symbol signal which is received when the principle wave is mixed with such a reflected wave and the sweep symbol signal which is previously stored in the receiver are shown in Figs. 12 and 13, respectively.

15 Fig. 12 shows the case of the transmission path condition in which both of the principle wave having a high level, and the reflected wave which has a level lower than that of the principle wave, but which brings a certain delay time are present. If the
20 principle wave is mixed with such a reflected wave, then the peaks which correspond to the levels and the delay times of the principle wave and the reflected wave are respectively generated in the cross-correlation value sequence of the receiver, respectively. In Fig. 12, the correlation peak brought by the principle wave is present at the center of the graph and the correlation peak brought by the reflected wave is present on the right-hand side thereof.

The correlation maximum value position detection unit 65 of the receiver detects the maximum value out of the cross-correlation value sequence as shown in Fig. 12.

5 In this case, since the correlation maximum value brought by the principle wave is present at the center of the graph, the correlation maximum value position detection unit 65 detects the correlation peak brought by the principle wave as the maximum value, and
10 on the basis thereof, carries out the reception sampling clock synchronous processing, and the control for the frame timing and the symbol timing.

Fig. 10 shows a schematic view of the received signal at this time. Also, Fig. 10 shows the
15 state in which the delay time of the reflected wave is shorter than the guard interval period of time.

In this case, since the correlation maximum value is brought by the principle wave having a high level, the time window of the FFT arithmetic operation
20 unit 69 is determined on the basis of the timing of the principle wave. Therefore, the principle wave is not mixed with the longitudinal symbol at all and hence no inter-symbol interface is generated.

On the other hand, Fig. 13 shows an example
25 in the case of the transmission path condition in which both of the principle wave, and the reflected wave having a level higher than that of the principle wave and also having a delay time shorter than the guard

interval length are present. The correlation peak brought by the principle wave is present at the center of the graph of Fig. 13, and also the correlation peak brought by the reflected wave having a higher level 5 than that of the principle wave is shown on the right-hand side of the graph.

In such a case, since as shown in Fig. 13, in the cross-correlation value sequence, the correlation peak brought by the reflected wave on the right-hand side of the graph is the maximum value, the correlation maximum value position detection unit 65 detects that correlation peak as the maximum value.

Accordingly, the control for the frame timing and the symbol timing is carried out on the basis of 15 the correlation peak brought by that reflected wave.

The state of the received signal in this case is shown in Fig. 14. In this case, since the frame timing and the symbol timing provided by the frame counter 82, as described above, is controlled on the basis of the reflected wave, the time window of the FFT arithmetic operation unit 69 is also determined on the basis of the timing of the reflected wave.

Thus, since the FFT time window is synchronized with the reflected wave, in addition to the principle wave of the current symbol and the reflected wave thereof, a part of the principle wave of a next symbol is composed into the reception sample value sequence signal which is in turn inputted to the FFT

arithmetic operation unit 69, and hence the inter-symbol interference will occur. In other words, since the principle wave of the current symbol is mixed with the principle wave of the next symbol in the form of 5 noise, as a result, the degradation of the C/N ratio is caused to degrade the code error rate.

Showing an example of this degradation of the C/N ratio, in the case where the effective symbol length is $51.2 \mu\text{sec}$, and also the principle wave of the 10 control symbol is mixed with the reflected wave which has a level higher than that of the principle wave by 5 dB and which has a delay time of $1.5 \mu\text{sec}$, there is given the disadvantage that the C/N ratio is degraded down to about 21 dB.

15 Next, Fig. 22 is a graphical representation showing the cross-correlation value sequence in the case of the transmission path condition in which both of the principle wave, and the reflected wave having a level higher than that of the principle wave and also 20 having a delay time longer than the guard interval length, are present.

The correlation peak brought by the principle wave is present at the center of the graph, and the correlation peak brought by the reflected wave having a 25 higher level than that of the principle wave is shown on the right-hand side of the graph.

In such a case, if the time window of the FFT arithmetic operation unit 69 is set in timing with the

reflected wave, then the degree of the inter-symbol interference may become less in some cases.

An example in such a case will hereinbelow be described with reference to a schematic view of Fig.

5 23, and Fig. 24.

In the case where as shown in Fig. 23, the FFT time window is set on the basis of the timing of the principle wave, the reflected wave of the current symbol is mixed with the reflected wave of the preceding symbol beyond the guard interval to cause the inter-symbol interference. On the other hand, in the case where the FFT time window is set on the basis of the timing of the reflected wave, since the principle wave of the current symbol is mixed with the principle wave of the next symbol, similarly, the inter-symbol interference is caused.

In other words, while when the principle wave of the current symbol is mixed with the reflected wave having a longer delay time than the guard interval length, the inter-symbol interference is caused either in the case where the FFT time window is set on the basis of the timing of the principle wave or in the case where the FFT time window is set on the basis of the timing of the reflected wave, the degree of the inter-symbol interference thus caused differs depending on whether the current symbol is mixed with the reflected wave of the preceding symbol or the current symbol is mixed with the next symbol of the principle

wave.

Fig. 24 is a diagram showing that, in order to obtain a less inter-symbol interference, the FET time window should be synchronized with which one of
5 the principle wave or a reflected wave when the reflected wave has a longer delay time than the guard interval length.

Now, the axis of ordinate shown in Fig. 24 represents the D (Desired)/U (Undesired) ratio of the
10 level of the principle wave to the level of the reflected wave in decibels, and the axis of abscissa represents the delay time of the reflected wave. In this connection, in this case, it is assumed that the
15 effective symbol length of the OFDM data symbol is 51.2 μ sec, and the guard interval length is 1.6 μ sec.

In this figure, it is shown that in the area (white part) of the upper part of the graph, the inter-symbol interference becomes less when the FFT time window is provided in the timing of the principle wave,
20 while in the area (oblique line part) of the lower part of the graph, the inter-symbol interference becomes less when the FFT time window is provided in the timing of the reflected wave. In addition, in the case where a level of the principle wave is higher than that of
25 the reflected wave when the delay time is within the guard interval, as described above, the time window of the FFT is always provided in timing with the principle wave, whereby the inter-symbol interference is not

caused at all.

Thus, when a reflected wave is present with the delay time longer than the guard interval length, the FET time window should be provided in timing with 5 which one of the principal wave or the reflected wave for a less inter-symbol interference depends on the delay time and the level of the reflected wave.

Now, taking the operation in the mobile transmission into consideration, as described above, 10 since the state of the transmission path is changing every moment, the cross-correlation value sequence is changed as shown in the examples of Figs. 12 and 13. For example, the correlation peak brought by the principle wave becomes large in a certain frame, while 15 the correlation peak brought by the reflected wave becomes large in the next frame, and so forth. Thus, the fluctuation of the correlation peak values of the principle wave and the reflected wave in the cross-correlation value sequence becomes violent.

20 As described above, since the correlation maximum value position detection unit 65 follows such a fluctuation of the cross-correlation value sequence, the position of the time window when detecting the maximum value changes depending on the state of the 25 transmission path, and the value of the error information ERR will also change.

This is reflected to the VCO control unit 66, and as a result, the reception sampling clock frequency

outputted from the VCO 67 is also changed so that the proper demodulation processing can not be carried out in the demodulation processing unit 6A.

In addition, since the fluctuation of the
5 error information ERR brings the fluctuation of the count value of the frame counter 68, there arises a problem that both of the frame timing and the symbol timing also fluctuate.

In the light of the foregoing, the present
10 invention is intended to solve the above-mentioned problems, and it is therefore an object of the present invention to provide an OFDM digital transmission method in which the inter-symbol interference is less and hence the C/N ratio is better and an apparatus
15 employing the same, and a method and an apparatus for receiving an OFDM signal.

It is another object of the present invention to provide an OFDM digital transmission method by which the processing of synchronizing a reception sampling
20 clock, and the control for the frame timing and the symbol timing can be suitably carried out, and an apparatus employing the same, and a method and an apparatus for receiving an OFDM signal.

It is still another object of the present
25 invention to provide an OFDM digital transmission method by which even when a cross-correlation peak value fluctuates in the operation of a mobile transmission apparatus or the like which undergoes the

fluctuating transmission path state, a reception sampling clock frequency can be synchronized with a transmission side sampling clock frequency to continue to supply stably a reception side sampling clock and an 5 apparatus employing the same, and a method and an apparatus for receiving an OFDM signal.

In order to attain the above-mentioned objects of the present invention, an OFDM data transmission apparatus according to one aspect of the 10 present invention includes a receiver which analyzes a cross-correlation value sequence signal acquired from an arithmetic operation between a received signal consisting of a principle wave, a reflected wave or a composite wave thereof and a predetermined synchronous 15 symbol signal to detect, out of one or more correlation peaks brought by the principle wave and/or the reflected wave, an effective correlation peak in which the symbol interference becomes minimum to carry out a reception sampling clock synchronous processing and the 20 control for the frame timing and the symbol timing of the receiver on the basis of the effective correlation peak thus detected.

According to one feature of the present invention, an effective correlation peak is detected in 25 which a value of a correlation peak is equal to or larger than a predetermined value, and the inter-symbol interference becomes minimum and on the basis of the effective correlation peak thus detected, a control

signal is generated in accordance with which the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are carried out.

5 According to another feature of the present invention, if the above-mentioned effective correlation peak can not be detected, then the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are
10 suspended to hold the control state right before the suspension.

According to a further feature of the present invention, the control is carried out on the basis of the above-mentioned effective correlation peak in such
15 a way that the reception sampling clock frequency is synchronized with the sampling clock on the transmission side.

More specifically, a receiver according to the present invention may operate such that an
20 arithmetic operation of the cross-correlation between the received signal and a predetermined synchronous symbol is carried out to acquire a cross-correlation value sequence signal; and out of the cross-correlation value sequence signal thus acquired, a plurality of
25 correlation peaks are detected which are derived by the principle wave or the reflected wave. Each of the magnitudes of the detected correlation peak values is compared with the magnitude of a predetermined value.

Then, if each of the magnitudes of the detected one or more correlation peak values is larger than that of the predetermined value, then one of them which has less inter-symbol interference is judged to be the effective 5 correlation peak, thereby detecting the correlation peak brought by the principle wave or the reflected wave having an electric power equal to or larger than a predetermined level.

Then, it is judged in timing with which of 10 the principle wave or the reflected wave the FFT time window may be provided in order to specify the correlation peak for establishment of synchronization.

On the basis of the effective correlation peak for establishment of synchronization acquired from 15 the above-mentioned processing, the the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are carried out.

Now, if the level of the effective correlation peak for establishment of synchronization which has been stably present till now is reduced so that the correlation peak value becomes smaller than the predetermined value, then it is judged that the state of the transmission path is of very poor quality and as 25 a result, the stable received signal has not yet reached the receiver. Then, the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are

suspended to carry out the demodulation while holding the control state obtained when the reception was stably carried out.

In such a manner, the reception sampling 5 clock synchronous processing and the control for the frame timing and the symbol timing of the receiver are carried out on the basis of the optimal correlation peak, whereby the inter-symbol interference can be suppressed and the degradation of the code error rate 10 can also be suppressed.

In addition, even when the state of the transmission path fluctuates in the operation of the mobile transmission or the like and hence the cross-correlation peak value fluctuates in the receiver, the 15 processing of synchronizing the reception sampling clock frequency can be executed on the basis of the stable effective correlation peak. Thus, the reception sampling clock frequency can be always synchronized with the transmission sampling clock frequency at all 20 times to continue to supply stably the reception sampling clock.

An OFDM data transmission apparatus according to another aspect of the present invention includes a receiver for carrying out an arithmetic operation of 25 the correlation between an OFDM signal containing therein at least one of a principle wave and a reflected wave received and a predetermined synchronous symbol signal, out of one or more correlation peaks

contained in a cross-correlation value sequence signal acquired from the arithmetic operation of the correlation, detecting an effective correlation peak brought by the principle wave, and on the basis of the effective correlation peak thus detected, carrying out the the reception sampling clock synchronous processing and the control for the frame timing and the symbol timing of the receiver.

In the operation of the OFDM data transmission in which the reflected wave having a delay time longer than the guard interval and having a high level can substantially be assumed to be absent, there exist no such reflected wave which when synchronization is made therewith, would provide a less inter-symbol interference. Therefore, by setting the FFT time window on the basis of the correlation peak brought by the principle wave, the inter-symbol interference can be either removed or substantially disregarded.

In this connection, as for technologies associated with the OFDM transmission, reference may be made to U.S. Serial No. 09/096454, Seiichi Sano et al. filed on June 11, 1998 entitled "DATA TRANSMISSION APPARATUS AND RECEIVING APPARATUS USING ORTHOGONAL FREQUENCY DIVISION MULTIPLEX MODULATION SYSTEM" and U.S. Serial No. 09/203564, Seiichi Sano et al. filed on December 2, 1998 entitled "SYNCHRONIZATION DETECTION METHOD FOR DATA TRANSMISSION APPARATUS AND DATA TRANSMISSION APPARATUS USING THE SAME". The disclo-

sures of these prior applications are hereby incorporated by reference herein.

BRIEF DESCRIPTION OF THE DRAWINGS.

The foregoing and other objects and advantages of the invention will be apparent from the following more particular description of the preferred embodiments of the invention as illustrated in the accompanying drawings wherein:

Fig. 1 is a block diagram showing a configuration of an embodiment of a receiver according to the present invention;

Fig. 2 is a wave form chart useful in explaining one example of an OFDM modulated signal;

Fig. 3 is a wave form chart useful in explaining one example of an OFDM symbol;

Fig. 4 is a wave form chart useful in explaining the structure of a transmission frame of the OFDM modulated signal;

Fig. 5 is a block diagram showing a configuration of a transmitter of one example in an OFDM transmission apparatus;

Fig. 6 is a block diagram showing a configuration of a receiver of one example in the OFDM transmission apparatus;

Fig. 7 is a graphical representation showing one example of the state of a cross-correlation value sequence signal;

Fig. 8 is a time chart useful in explaining the operation of a frame counter 68 shown in Fig. 6;

Fig. 9 is a schematic diagram useful in explaining a time window of an FFT arithmetic operation 5 unit 69;

Fig. 10 is a schematic diagram useful in explaining the situation of mixing of a reflected wave within a guard interval period of time;

Fig. 11 is a schematic diagram useful in 10 explaining the situation of mixing of a reflected wave out of a guard interval period of time;

Fig. 12 is a graphical representation showing the state of a cross-correlation value sequence signal when a principle wave is mixed with a reflected wave 15 (having a low level);

Fig. 13 is a graphical representation showing the state of a cross-correlation value sequence signal when a principle wave is mixed with a reflected wave (having a high level);

20 Fig. 14 is a schematic diagram useful in explaining an FFT time window when synchronized with a reflected wave;

Fig. 15 is a block diagram showing an example of a configuration of an effective correlation position 25 detection unit 1 of the embodiment shown in Fig. 1 of the present invention;

Fig. 16 is a block diagram showing an example of a configuration of an effective correlation peak

detection unit 11 of the embodiment shown in Fig. 1 of the present invention;

Fig. 17 is a schematic diagram useful in explaining a cross-correlation value sequence $C(T)$;

5 Fig. 18 is a graphical representation showing
an example of a state of a cross-correlation value
sequence signal;

Fig. 19 is a block diagram showing an example of a configuration of a control state protection unit 10 12 of the embodiment shown in Fig. 1 of the present invention:

Fig. 20 is a graphical representation showing a state of a cross-correlation value sequence signal in which a correlation peak brought by a principle weave 15 does not exceed a predetermined value;

Fig. 21 is a timing chart useful in explaining the operation of the control state protection unit 12 of the embodiment shown in Fig. 1 of the present invention:

20 Fig. 22 is a graphical representation showing
an example of a state of the cross-correlation value
sequence signal;

Fig. 23 is a schematic diagram representing an FFT time window when a principle wave is mixed with a reflected wave; and

Fig. 24 is a graphical representation showing that does the inter-symbol interference become less when with which of a principle wave or a reflected wave

the synchronization is made.

DESCRIPTION OF THE EMBODIMENTS

A digital transmission according to an embodiment of the present invention will hereinafter be 5 described in detail with reference to the accompanying drawings. In this connection, in the figures, the same parts are designated with the same reference numerals.

Fig. 1 is a block diagram showing a configuration of a receiver of a digital transmission 10 apparatus according to one embodiment of the present invention.

In Fig. 1, a received signal transmitted from a transmitter like one shown in Fig. 5 to reach the receiver through a transmission path is first converted 15 from a signal having a inter frequency (IF) band to a signal having a base band frequency band in an IF/BB conversion unit 61, as described with reference to Fig. 6.

An output signal from the IF/BB conversion 20 unit 61 is subjected to the analog/digital conversion in an A/D conversion unit 62 using a reception sampling clock. A reception sample value sequence signal acquired from the A/D conversion unit 62 is inputted to a null symbol detection unit 63, a sweep symbol 25 correlation arithmetic operation unit 64 and an FFT arithmetic operation unit 69. The null symbol detection unit 63 detects a null symbol from the reception

sample value sequence signal to detect roughly a starting point of a frame. An output signal NS from the null symbol detection unit 63 is inputted to the sweep symbol correlation arithmetic operation unit 64

5 and then the arithmetic operation of the cross-correlation between the reception sample value sequence signal and a sweep symbol which is previously set is carried out in timing with the frame starting signal NS to acquire a cross-correlation value sequence.

10 Description will hereinbelow be given with respect to the operation of the receiver including an effective correlation position detection unit 1 according to the present invention.

15 Fig. 15 is a block diagram showing a configuration of the effective correlation position detection unit 1. The effective correlation position detection unit 1 is constituted by an effective correlation peak detection unit 11 and a control state protection unit 12. In addition, the detailed configuration of the effective correlation peak detection unit 20 11 is shown in Fig. 16.

A cross-correlation value sequence signal as an output signal from the sweep symbol correlation arithmetic operation unit 64 is inputted to a DFF (a D-25 type flip-flop) 114 an output signal of which is in turn inputted to a DFF 115. Now, if the cross-correlation value sequence signal as shown in Figs. 7, 12 and 13, and the like, as shown in Fig. 17, is

defined as $C(T)$ (but, T is a sample number and is one of natural numbers), then the input signal to the DFF 114, the input signal to the DFF 115 and the output signal from the DFF 115 can be expressed in the form of $C(T)$,

5 $C(T - 1)$ and $C(T - 2)$, respectively.

As described above, by the principle wave in the received signal is meant the signal which reaches earliest the receiver. Thus, the correlation peak at the earliest time point, out of the correlation peaks,

10 in the cross-correlation value sequence $C(T)$, i.e., at a time point when T is smallest is the correlation peak brought by the principle wave, and also the correlation peak following that correlation peak is brought by the reflected wave.

15 The fact that the peaks are present in the cross-correlation value sequence $C(T)$ means that if the differential coefficient $(dC(T)/dT)$ of $C(T)$ is increased as T is increased, and after the maximum value of the peaks, the differential coefficient of $C(T)$ has a

20 tendency to be decreased, then it follows that the peak is present, and the maximum value of the peak at that time is given as the peak value.

If this fact is expressed in the form of the sample value sequence, since the differential coefficient is expressed by $\{C(n) - C(n - 1)\}$ (n : natural numbers), when the following relations are established, $C(T - 1) - C(T - 2) > 0$ (a differential coefficient has a tendency to be increased) ... (1)

and $C(T) - C(T - 1) < 0$ (a differential coefficient has a tendency to be decreased) ... (2)
it can be said that the peak is present in the cross-correlation value sequence signal, and also the peak
5 value at this time is $C(T - 1)$.

Describing the above-mentioned expression (1) on the basis of the configuration of the effective correlation peak detection unit 11, $C(T - 2)$ as the output signal from the DFF 115 is subtracted from $C(T - 10) 1)$ as the output signal from the DFF 114 in a subtracter 117.

The subtracter 117 carries out the subtraction of $C(T - 1) - C(T - 2)$ to output the most significant code bit of the subtraction result in order 15 to show whether the result of the arithmetic operation is a positive number or a negative number. When the subtraction is carried out using the 2s complement, if the code bit is 0, then it is shown that the subtraction result is a positive number, while if the code bit 20 is 1, then it is shown that the subtraction result is a negative number.

In addition, likewise, describing the above-mentioned expression (2) on the basis of the configuration of the effective correlation peak detection unit 25 11, $C(T - 1)$ as the output signal from the DFF 114 is subtracted from $C(T)$ as the input signal to the DFF 114 in a subtracter 116. This subtracter 116 carries out the subtraction of $C(T) - C(T - 1)$ to output similarly

the code bit exhibiting whether the result of the arithmetic operation is positive or negative.

Now, since the presence of the peak is acquired when the expressions (1) and (2) are both 5 established at the same time, it is established when the subtraction result of the subtracter 117 is a positive number, i.e., the logical value of the output from the subtracter 117 is 0, and also the subtraction result of the subtracter 116 is a negative number, i.e., 10 the logical value of the output from the subtracter 116 is 1.

Next, an output signal from the subtracter 117 is inputted to an inverter 118 in which the logic of the signal is in turn inverted to be inputted to one 15 input terminal of an AND circuit 119. An output signal from the subtracter 116 is inputted to the other input terminal of the AND circuit 119. Then, when the logical values of the two input signals are both 1s, i.e., the correlation peak is present, the AND circuit 20 119 outputs an output signal having a logical value of 1, and otherwise, outputs an output signal having a logical value of 0.

However, in the cross-correlation value sequence which is shown in Figs. 7, 12 and 13, and the 25 like, with respect to the correlation peaks which are detected on the basis of the above-mentioned processings, in parts as well in each of which the level of the wave form of the cross-correlation value sequence

is small, a large number of correlation peaks are present. Those correlation peaks each having a low level are not the correlation peaks each of which is generated when the time window of the arithmetic 5 operation of the cross-correlation coincides with the sweep symbol of the principle wave or the reflected wave, but are generated due to the noises.

Therefore, in order to remove any of the correlation peaks due to the noises, as shown in Fig. 10 18, a predetermined value is set in the cross-correlation value sequence and then the correlation peak is judged to be the effective correlation peak when the value of the correlation peak is equal to or larger than the predetermined value. In such a way, a 15 plurality of effective correlation peaks brought by the principle wave or the reflected wave are detected from within the acquired cross-correlation value sequence.

Describing this operation, this predetermined value is outputted from a threshold generator 111. The 20 predetermined value is either previously set to a fixed value or set to an arbitrary fraction of the level of the reception sample value sequence to make follow the level of the reception sample value sequence.

The output signal from the threshold 25 generator 111 is inputted to a minus input terminal of a comparator 112. In addition, to a plus input terminal of the comparator 112 is inputted $C(T - 1)$ as the value of the correlation peak, i.e., an output

signal from the DFF 114. The comparator 112 compares the magnitude of the output value of the DFF 114 with the magnitude of the output value from the threshold generator 111, and when the magnitude of the output 5 value from the DFF 114 is larger than the magnitude of the output value from the threshold generator 111, outputs the logical value of 1 to show that the correlation peak of interest is the effective correlation peak.

10 With the arrangement, the effective correlation peak is acquired when both of the logical values of the output signal from the AND circuit 119 as the flag exhibiting that the correlation peak is present and the output signal from the comparator 112 15 as the flag exhibiting that the correlation peak has a predetermined level and hence is effective are both 1s.

Now, the output terminal of the AND circuit 119 is electrically connected to one input terminal of the AND circuit 113, and the output terminal of the 20 comparator 112 is electrically connected to the other input terminal of the AND circuit 113. As a result, when both of the logical values of the two input signals to the AND circuit 113 are 1s, the AND circuit 113 outputs the logical value of 1 as a VPK signal, and 25 when 1 is outputted therefrom, it is shown that there is the effective correlation peak.

In addition, in the above-mentioned correlation peak detection processings, a cross-correlation

00020000000000000000000000000000

value sequence counter 11A counts a sample number T of the cross-correlation value sequence, and when the count values of the corresponding correlation peaks, i.e., a plurality of effective correlation peaks are 5 present, outputs the respective sample number Ts.

Each of the above-mentioned VPK signals is inputted to a PK terminal of an interference discrimination unit 11C, and the output signal from the DFF 114 at that time, i.e., each of the corresponding correlation peak values is inputted to a DATA terminal of the interference discrimination unit 11C, and also the output signal from the correlation value sequence counter 11A at that time, i.e., each of the corresponding sample numbers is inputted to an LOC terminal 10 15 of the interference discrimination unit 11C.

The interference discrimination unit 11C discriminates that, in order to obtain a less inter-symbol interference the FET time window should be provided in synchronism with which one of the principle 20 wave or the reflected wave constituting the received signal, and choose the correlation peak in which the inter-symbol interference is least as the correlation peak for establishment of synchronization.

For example, as seen from Fig. 24, when the 25 delay time of the reflected wave falls within the guard interval, the inter-symbol interference becomes less when the synchronizatin is made with the principle wave, no matter what the D/U ratio is. However, when a

reflected wave is present the delay time of which exceeds the guard interval, it can be discriminated from Fig. 24 that it may be better to provide the FET time window in synchronism with which one of the 5 principle wave or the reflected wave on the basis of the D/N ratio.

Next, the operation of the interference discrimination unit 11C will hereinbelow be described in detail.

10 The interference discrimination unit 11C judges that when the logical value at the PK terminal becomes 1 as described above, each of the correlation peak values at the DATA terminal and each of the sample number at the LOC terminal are valid, and stores those 15 values in memory means such as a RAM (Random Access Memory) or an FF (Flip-Flop)(not shown). In other words, for example, in the case as shown in Fig. 18, the two effective correlation peak values brought by the principle wave and the reflected wave, respectively, and the corresponding sample numbers are all 20 stored therein.

Then, the level difference (the D/U ratio) between the principle wave and the reflected wave is arithmetically operated on the basis of those effective 25 correlation peak values. As for the method of operating arithmetically the D/N ratio, the division between the level of the principle wave and the level of the reflected wave is carried out, and the logarithmically

arithmetic operation is carried out for the division result, whereby it is possible to operate arithmetically the D/U ratio. In addition, the sample number of the principle wave is subtracted from the sample number 5 of the reflected wave to operate arithmetically the delay time in sampling clocks.

Thus, by using the relation between the arithmetically operated D/U ratio and the delay time shown in Fig. 24, it is judged that, in order to obtain 10 a less inter-symbol interference the FET time window should be in synchronism with which one of the correlation peak of the principle wave or that of the reflected wave, and then on the basis of the judgement result, the correlation peak in which the inter-symbol 15 interference is least is made the correlation peak for establishment of synchronization.

However, the arithmetic operation circuit for carrying out the arithmetic operation for the correlation peak values brought by the principle wave and the 20 reflected wave, and the delay time to discriminate the condition shown in Fig. 24 requires a very large circuit scale. For this reason, the method is easier wherein it is previously arithmetically operated that does the inter-symbol interference become less when 25 with which of the principle wave or the reflected wave the synchronization is made in correspondence to the correlation peak values brought by the principle wave and the reflected wave, and the delay time, and this

arithmetic operation result is stored in memory means such as a RAM to carry out the discrimination.

As described above, the interference discrimination unit 11C discriminates that which one of 5 the principle wave or the reflected wave the synchronization should be attained with.

However, in the actual transmission path, it does not occur frequently that the reflected wave, as shown in the oblique line part of Fig. 24, which has a 10 long delay time and which has a high level is regularly present. In addition, when carrying out an OFDM system design, the design is in general carried out such that the delay time of the reflected wave due to the used frequency band and the transmission path environment 15 does not exceed the guard interval. In such a manner, when it is assumed that the reflected wave is not present such that when the synchronization is made with the reflected wave, the inter-symbol interference becomes less, a large number of redundant circuits are 20 included in the above-mentioned interference discrimination unit 11C.

For this reason, if out of a plurality of correlation peaks acquired in the interference discrimination unit 11C, the correlation peak having 25 the smallest sample number was discriminated as the correlation peak brought by the principle wave, and the FFT time window was provided on the basis of that correlation peak, then the inter-symbol interference

can be removed.

A circuit for realizing this is very simple in configuration. Thus, the smallest sample number may be detected out of a plurality of acquired sample 5 numbers using a comparator or the like. This circuit has an advantage that the circuit configuration thereof can be remarkably simplified as compared with that of the interference discrimination unit 11C as described above.

10 In addition, the interference discrimination unit 11C outputs as a VLOC the sample number when the effective correlation peak is present and also outputs the logical value of 1 to a flag (PKF) exhibiting that the effective correlation peak is present.

15 On the other hand, when the effective peak is absent in the cross-correlation value sequence and hence the logical values of all of the VPK signals are 0s, the interference discrimination unit 11C similarly outputs the logical value of 0 as the PKF.

20 The VLOC signal which has been outputted from interference discrimination unit 11C and which exhibits the sample number of the effective correlation peak is inputted to a position correction circuit 11B.

25 The position correlation circuit 11B, from this VLOC signal, i.e., from the sweep symbol position for establishment of synchronization, arithmetically operates the frame starting timing to output an error signal MERR against the count value, of the frame

starting timing, which has been counted in reception sampling clocks. Now, if the frame starting timing provided by the frame counter 68 coincides with the frame starting timing which is assumed from the sweep 5 symbol position for establishment of synchronization, then the logical value of the error signal MERR becomes 0, while if the error occurs, then the information relating to the error amount in sampling clocks is outputted.

10 By executing the above-mentioned processings, the effective correlation peak detection unit 11 detects the correlation peak in the cross-correlation value sequence to discriminate the correlation peak in which the inter-symbol interference is least. If the 15 correlation peak is present, then the effective correlation peak detection unit 11 outputs the error signal MERR exhibiting an error between the PKF signal as the flag exhibiting that the effective correlation peak is present and the count value of the frame 20 counter 68.

Next, a configuration of the control state protection unit 12 is shown in Fig. 19, and the operation thereof will hereinbelow be described.

As described above, in the operation in the 25 mobile transmission, the fluctuation of the correlation peak values of the principle wave and the reflected wave in the cross-correlation value sequence may become violent, and then the fluctuation of the reception

sampling clock frequency, and the fluctuation of the frame timing and the symbol timing may occur in some cases.

When the state of the transmission path is stable, the stable reception sampling clock is supplied to the receiver, both of the frame timing and the symbol timing are also stable, and the principle wave having a high level stably reach the receiver, the control state protection unit 12 operates in such a way that the effective correlation peak brought by the principle wave is made the correlation peak for establishment of synchronization in the receiver, and on the basis of this effective correlation peak, the control for the reception sampling clock frequency, and the control for the frame timing and the symbol timing are carried out.

On the other hand, when the state of the transmission path is of very poor quality and hence the stable principle wave does not reach the receiver, the control state protection unit 12 has the function of suspending the above-mentioned control in the receiver and carrying out the demodulation while maintaining the state experienced when the principle wave stably reaches the receiver.

This operation of the control state protection unit 12 will hereinbelow be described in detail with reference to a timing chart shown in Fig. 21.

When the synchronization is unestablished,

the error information MERR outputted from the effective correlation peak detection unit 11 fluctuates largely, and hence the control for the reception sampling clock frequency and the control for the frame timing and the 5 symbol timing are carried out.

Thereafter, when the synchronization is established and the state of the transmission path also becomes stable, the fluctuation of the error information MERR becomes less (e.g., the fluctuation amount 10 falls within ± 1).

A comparator 121, when the inputted error information MERR falls within a predetermined range (e.g., ± 1), exhibits the stable reception state to output the logical value of 1.

15 However, when the state of the transmission path which has been stable till now fluctuates to bring the cross-correlation value sequence as shown in Fig. 20, and the correlation peak value of the principle wave in the comparator 112 shown in Fig. 16 becomes 20 smaller than a level of the threshold generator 111, the fluctuation of the error information MERR becomes abruptly large, and also the value of the error information MERR exceeds a predetermined range (e.g., ± 1). At this time, the comparator 121 exhibits that the 25 state of the transmission path fluctuates and becomes unstable to output the logical value of 0.

In addition, PKF as the flag exhibiting that the effective correlation peak is present is inputted

to one input terminal of an AND circuit 122. An output signal from the comparator 121 is inputted to the other input terminal of the AND circuit 122. When the two conditions are established that PKF is 1, i.e., the 5 effective correlation peak is present, and the logical value of the output signal of the comparator 121 is 1, i.e., the state of the transmission path is stable, the AND circuit 122 outputs the logical value of 1.

An output signal from the AND circuit 122 is 10 inputted to a U/D terminal of the updown counter 124. The updown counter 124 up-counts the count value when the logical value of the signal at the U/D terminal is 1, while down-counts the count value when the logical value of the signal at the U/D terminal is 0.

15 After the updown counter 124 counts the count value up to the value outputted from a counter upper limit value generator 123 (in Fig. 21, an output value thereof is set to 10 for example), it holds the count value for a period of time ranging from that time point 20 (t1) to a time point when the logical value of 0 is inputted to the U/D terminal.

In such a manner, the fact that the count value is held at the value in the counter upper limit value generator 123 means that the state of the 25 transmission path is within a period of time from t1 to t2 when it is regularly stable.

An output signal from the updown counter 124 is inputted to one input terminal of a comparator 126,

and an output terminal of a protection value generator 125 is electrically connected to the other input terminal of the comparator 126.

The comparator 126 compares the magnitude of
5 an output signal from the updown counter 124 with the magnitude of a predetermined value which is set in the protection value generator 125, and outputs the logical value of 1 when the value of the updown counter 124 is larger than the value of the protection value generator
10 125, while outputs the logical value of 0 when the value of the updown counter 124 is smaller than the value of the protection value generator 125.

In addition, the value of the protection value generator 125 is previously set to a value
15 smaller than that of the counter upper limit generator 123 (in the case of Fig. 21, it is set to 5 for example).

When the state of the transmission path is in the stable state as for a period of time from t_1 to t_2 ,
20 since the count value of the updown counter 124 is larger than that of the protection value generator 125, the comparator 126 outputs the logical value of 1.

The output signal from the comparator 126 is inputted to one input terminal of the AND circuit 129, 25 and the signal which has been acquired by inverting the logic of the output signal from the AND circuit 122 in an inverter 128 is inputted to the other input terminal of the AND circuit 129.

Therefore, since for a stable period of time from t_0 to t_2 , the logical value of the output signal from the AND circuit 122 is 1, the logic of the input signal to the AND circuit 129 is inverted in the 5 inverter 128 to be 0, and hence the logical values of the two input signals to the AND circuit 129 become 1 and 0, respectively, so that the logical value of the output signal from the AND circuit 129 becomes 0.

An output terminal of the AND circuit 129 is 10 electrically connected to a switching terminal of a selector 12A. Then, the selector 12A, when the logical value of the signal at the switching terminal is 0, outputs a signal at an I0 terminal as the error information signal ERR and when the logical value of 15 the signal at the switching terminal is 1, outputs a signal at an I1 terminal.

Therefore, since for a period of time from t_0 to t_2 , the logical value of the input signal at the switching terminal is 0, the selector 12A outputs as it 20 is the signal at the I0 terminal, i.e., the error signal MERR as the error information ERR to apply the error information ERR to the VCO control unit 66 to control the VCO 67 in such a way that the reception sampling clock frequency is synchronized with the 25 sampling clock frequency on the transmission side.

However, when the state of the transmission path fluctuates from the regularly stable state to the unstable state in an instant (for a period of time from

t₂ to t₃), the logical value of the output signal from the AND circuit 122 exhibiting the state of the transmission path becomes 0, and hence the updown counter 124 starts to carry out the down-count. However, in 5 this case, since the count value of the updown counter 124 is larger than the value of the protection value generator 125, the comparator 126 outputs the logical value of 1.

Then, in this case, since the logical value 10 of the output signal from the AND circuit 122 becomes 0 to be inverted in the inverter 128, the logical value of the input signal to the other input terminal of the AND circuit 129 becomes 1, and hence the AND circuit 129 outputs the logical value of 1.

15 As a result, on the basis of the output signal having the logical value of 1 from the AND circuit 129, the terminal of the selector 12A is switched over to the I1 terminal side so that the selector 12A outputs as the error information signal 20 ERR an output signal having the logical value of 0 from a zero-value generator 127 in accordance with which the logical value of the error information signal ERR which is used to control the VCO 67 is made 0.

At the time when the logical value of the 25 error information ERR becomes 0, the VCO control unit 66, on the assumption that the reception sampling clock frequency error is absent, holds the frequency-controlled voltage of the VCO 67 at the current value.

In such a manner, when the situation of the transmission path fluctuates in an instant from the regularly stable state to the unstable state, the demodulation operation is carried out while holding the 5 control state exhibited when the reception has been stably carried out.

Then, for a period of time from t_3 to t_4 when the state of the transmission path is stable, the same processing as that for a period of time from t_0 to t_2 10 is executed to output as the error information the signal MERR as it is.

Next, description will hereinbelow be given with respect to the case where the state of the transmission path becomes continuously unstable as for a 15 period of time from t_4 to t_6 .

First, for a period of time from t_4 to t_5 when the output value from the updown counter 124 is larger than the value of the protection value generator 125 and hence the comparator 126 outputs the logical 20 value of 1, the same processing as that for a period of time from t_2 to t_3 is executed, and the logical value of the error information signal ERR is made 0 to hold the current control state.

However, at the time when the magnitude of 25 the output signal from the updown counter 124 becomes smaller than the value of the protection value generator 125 (at a time t_5), the logical value of the output signal from the comparator 126 becomes 0, and

the logical value of the AND circuit 129 also becomes 0.

Therefore, during a period of time from t_5 to t_6 , the terminal of the selector 12A is switched over 5 to the I0 terminal side, and hence the selector 12A outputs as the error information ERR the inputted signal MERR as it is.

That is, for this operation, when the situation of the transmission path becomes continuously 10 unstable for a longer period of time than the value (a period of time) which is set in the protection value generator 125, since the possibility that the state of the control for the receiver is not synchronized with the transmission side is high, the control for the 15 reception sampling clock frequency, and the control for the frame timing and the symbol timing are both carried out again.

While in the receiver according to the present invention as has been described above, both of 20 the frame timing and the symbol timing are controlled on the basis of the correlation peak for establishment of synchronization, the function of the present invention may also be attained in such a way that only the FFT time window is shifted in the direction of the 25 time base while stabilizing the control for the frame timing and the symbol timing.

In addition, while in the above-mentioned embodiment, the sweep symbol is employed as the

synchronous symbol which is used to carry out the cross-correlation arithmetic operation, it is to be understood that even if the sweep symbol is replaced with any of other suitable signals, the present

5 invention may also be implemented.

For example, as the method of modulating the data symbol, there is known the differential wave detection method wherein the phase difference between the signal of interest and the signal one symbol before 10 the signal of interest is detected, and the demodulation is carried out in accordance with the phase difference. When the differential wave detection method is employed, the reference signal exhibiting the initial phase reference thereof is required, and this 15 reference signal is referred to as the reference symbol.

With respect to the reference symbol, the random phase reference signals are provided for all of the carriers, respectively, those signals are subjected 20 to the IFFT processing similarly to the data symbol to add the guard interval thereto. The reference symbol is arranged as the synchronous symbol in the synchronous symbol group of the frame heads. Since it is general that the reference symbol employs the same 25 signal every frame, the wave form of the reference symbol can be previously acquired by using a computer or the like. In such a manner, the arithmetic operation of the cross-correlation between the known

reference symbol and the received signal sequence is carried out, whereby similarly to the sweep symbol, the control for the FFT time window position and the control for the VCO frequency can also be carried out.

5 As set forth hereinabove, in the receiver according to the above-mentioned embodiment, even in the case where the state of the transmission path is of very poor quality and hence the composite signal of the principle wave and the reflected wave is received as

10 the received signal, and also the level of the reflected wave becomes larger than that of the principle wave, the control for the frame timing and the symbol timing, i.e., the control for the time window of the FFT arithmetic operation is carried out

15 in such a way that the inter-symbol interference becomes minimum, whereby it is possible to suppress the degradation of the code error rate.

In addition, in the case where the state of the transmission path fluctuates in the operation of

20 the mobile transmission or the like and hence the correlation peak value in the receiver fluctuates, when the state of the transmission path is of very poor quality, and hence the stable principle wave does not yet reach the receiver, the control for the reception

25 sampling clock frequency is suspended to hold the state obtained when the stable reception is carried out, whereby it is possible to continue to supply stably the reception sampling clock.

While the invention has been particularly described and shown with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail and omission may be made therein without departing from the scope of the invention.